

Spiral Inductor Performance in Deep-Submicron Bulk-CMOS with Copper Interconnects

William B. Kuhn, Aaron W. Orsborn, Matthew C. Peterson, Shobak R. Kythakyapuzha, Aziza I. Hussein
Jun Zhang, Jianming Li, Eric A. Shumaker, and Nandakumar C. Nair

Department of Electrical and Computer Engineering, Kansas State University, Manhattan, KS 66506, USA

Abstract This paper reviews design considerations for spiral inductors in bulk CMOS and reports investigations carried out in a commercial 0.18 μm process using 6-layer copper metallization. Quality factors of approximately 8 are measured for 10nH spirals operating between 1 and 2 GHz. Comparisons of Q and self-resonant frequency are provided for a variety of construction variables including with/without a patterned ground shield, metal-6 only versus stacking layers 3 thru 6, dense versus sparse vias, wide versus narrow traces, and with/without metal-fill.

I. INTRODUCTION

Many studies of spiral inductor performance in bulk CMOS processes have been published in the past decade (e.g. [1,2]), but each typically concentrates on a selected set of issues such as optimum trace width and gap or substrate losses, while only briefly acknowledging others such as current-crowding. Still other issues have not yet received adequate attention, including via density when stacking metal layers, or the effects of fill-metal on performance, leaving designers to make educated guesses in these areas. This paper attempts to address all of these issues by comparing an array of spirals fabricated in a modern deep-sub-micron, bulk CMOS process representative of those which will support system-on-a-chip developments in the coming years.

II. DESIGN CONSIDERATIONS

Figure 1 illustrates the basic issues determining the three most important spiral inductor performance parameters: inductance (L), self-resonant-frequency (SRF), and quality factor (Q). Inductance is primarily determined by the spiral's dimensions, including its size (D), trace width (W), and number of turns (N). SRF is also determined by these parameters in conjunction with turn-to-substrate capacitances (C_{ts}) -- although to a lesser extent, trace-to-trace fringe and sidewall capacitance, and substrate resistances R_s , are also factors. In this paper, spiral inductors with $D = 350\mu\text{m}$, $N=6$, and $W=10$ to $17\mu\text{m}$ yield nominal inductances of approximately 10 nH, while variations in C_{ts} determined by trace width and other factors lead to SRF values between 1.7 and 2.7 GHz.

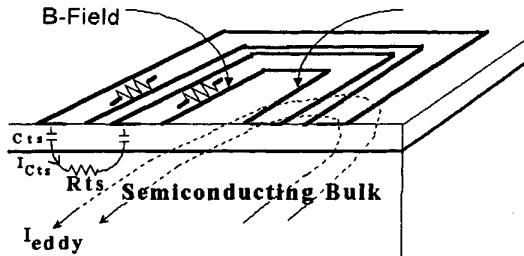


Figure 1. Perspective view of spiral inductor showing important factors determining L, SRF, and Q.

Inductor Q is a somewhat more complex issue and its optimization is a primary goal of most designers. To a first order, Q is determined at low frequencies by the ratio of inductive reactance (X_L) to the DC series resistance (R_{dc}) of the thin metal traces in which the spiral is fabricated. This leads to the obvious approach of paralleling multiple metalization layers [2] (although at the expense of a modest decrease in SRF from an attendant increase in C_{ts}), and to the desire for lower resistance metalizations such as copper [3]. In this paper, copper metallization is employed and most spirals are constructed by paralleling metal layers 3 thru 6, leading to good Q values (> 5) at frequencies as low as 500 MHz. As higher frequencies are approached, however, three factors¹ conspire to degrade Q and prevent it from following the expected linear increase suggested by X_L/R_{dc} :

- I^2R loss from currents I_{Cs} flowing through substrate resistance R_s ,
- I^2R losses from eddy currents induced deep within the substrate below the spiral traces, and
- I^2R losses from eddy currents in the metal traces themselves.

The first of these problems can be addressed by placing a ground-shield between the traces and the substrate [4,5]. This shield effectively decreases R_s and hence associated power losses, leading to improved Q. This proven method of optimizing Q is employed in most spirals in this study, although one spiral is created without a shield to demonstrate its effect.

The second problem is primarily an issue in CMOS processes that employ epi-wafers with a low resistivity

¹ Classic skin-effect should be considered, but is small for metal $< 2\mu\text{m}$ thick at $f < 2$ GHz, and is not included here.

substrate bulk (0.01 to 0.02 Ohm-cm) to mitigate latchup. Many modern processes, including that used here, employ non-epi wafers with resistivities in the range of 20 Ohm-cm. For such processes, the circulating eddy currents can be shown to be negligible [5], and this issue is not considered in this paper.

The last problem is perhaps the most severe, especially for multi-turn spirals. The spiral's B-field generated by nearby turns passes perpendicularly through the traces, setting up eddy currents and pushing currents to the trace edges[6]. The result is a quadratic increase in resistance with frequency, with the frequency of on-set determined by trace width, pitch, and sheet resistance[7]. Studies of this problem indicate that narrower traces may be helpful, since the areas of the eddy loops are reduced. Studies also predict that use of lower resistance in the traces increases the severity of the problem, which unfortunately leads to diminishing returns for paralleling metal traces or application of low-R metals. To validate these predictions, spirals are included in this study which have narrow traces, and which use only top-layer metal.

Finally, the introduction of newer, deep-submicron processes with small metal pitch bring their own difficulties. Such processes often use fabrication techniques that demand the use of fill-metal in locations where metal density is below some minimum value. The impact of this fill metal is also studied in this paper.

III. REFERENCE INDUCTOR DESIGN

The reference inductor to which all variations in our array will be compared is shown at the right-hand side of figure 2. Also shown in this photo are the inductors without metal-fill (center) and with narrow traces (left). The outside turn of the reference inductor measures 350 um on a side, and the trace width is approximately 17 um, with a gap between turns of 4um. Metals 3 through 6 are paralleled with stacked vias with a via-to-via pitch on the order of 1um, giving approximately 200,000 vias! Sheet resistance for the combined layers is 0.013 Ohm/sq.

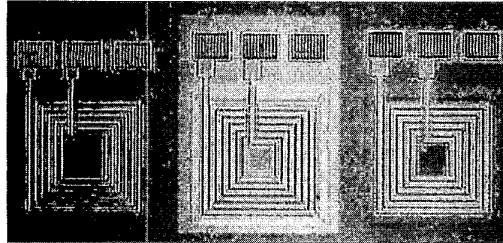


Figure 2. Photo of three of the spirals in the array.

A patterned ground shield built from 8 Ohm/sq poly is placed below the spiral and a 28um wide ground ring of paralleled metals 1,2 contacts the outer edge of the shield and connects with the inductor's outer turn at the probe pad (upper left of the spiral). Simulation software [8,9] was used to confirm that the resistance of this ground ring is sufficiently small to avoid significant degradation of Q.² The ground contact ring is broken at the lower right to avoid setting up circulating currents. To minimize eddy current loops within the shield itself, the shield is patterned, as done by Yue, et.al [4], using cuts at right angles to the traces every 10um

IV. MEASUREMENTS

All measurements were made with an HP/Agilent 8753E network analyzer and ECP18 GSG PicoProbes after calibrating using a Cascade Microtech impedance substrate. Calibration accuracy was checked on the short, open, load references and an open-circuit line provided on the substrate. DC contact resistance was also measured using a shorted probe pad structure included on the chip, and found to be negligible (< 0.2 Ohms). Raw S11 measurements of the reference spiral from 0 to 6 GHz are shown in Figure 3. Marker 1 shows a DC resistance of 4.3 Ohms, while marker 4 indicates an SRF of 1.70 GHz.

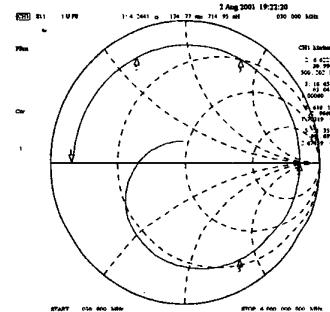


Figure 3. Measured S11 of reference spiral.

S11 measurements of the inductors were then fit to a simple model consisting of a series R and L, with a parallel C placed across this series combination [7]. While more complex 'PI' type models are employed by many authors, these models originated from the desire to model substrate resistance (Rts) effects, and are not needed here due to the use of a ground shield. The series-RL, shunt-C model used in this work provides a more direct representation of effects of the remaining Q degradation mechanisms (e.g. current-crowding).

The series-RL, shunt-C model was fit to the data by converting S11 to an admittance Y, subtracting off the susceptance of C (found from L measured at low frequency

² A first prototype used a 5um wide ground contact ring of metal 1 only, leading to significant Q degradations.

and SRF), and then converting this Y' value to Z' , which gives the RL values (from its real and imaginary parts). The inductor Q can then be found simply from X_L/R .³ As a test of the validity of this simple model, L, computed from X_L/ω , can be plotted versus frequency and checked to confirm it is relatively constant. This was done in this study for all spirals in the array, including that without a ground shield, and the L values were found to vary by less than 5% to well above the SRF.

The extracted Q and L values for the reference spiral up to SRF are shown in Figure 4, together with the series resistance variation. This series resistance variation is also compared to analytically predicted results using the formulas in [7]. Note that the measured Q has reached a respectable 5 even at 500 MHz, thanks to the low resistance copper metalization and the paralleling of layers 3 through 6. However, at high frequencies, Q begins to decrease due to current-crowding.

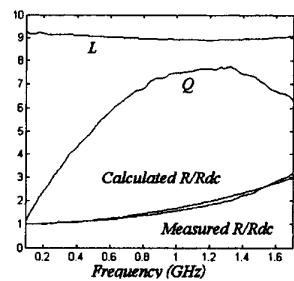


Figure 4. Performance of reference spiral.

V. METAL THICKNESS AND TRACE WIDTH

Analysis of current crowding predicts that the critical frequency where R/R_{dc} reaches 1.1 is a function of both trace sheet resistance and trace width [7]. To validate the first dependence, a spiral was constructed identical to the reference inductor, but using metal-6 only, giving $R_{sheet} = 0.05$ Ohms/sq. The results are shown in the left-hand plot of figure 5. As expected, Q is significantly degraded at low frequencies due to the higher sheet resistance, but current-crowding in this spiral does not begin until almost 2 GHz. Hence, Q at high frequencies nearly equals that for the reference spiral with 4x lower sheet R. Note also that the SRF is increased to approximately 2.2 GHz due to the additional oxide thickness available when only top-metal is employed.

Studies of inductor performance versus trace width have led some authors to conclude that traces should be made as wide as possible, while others recommend against this. This confusion can be solved by looking at the

³ Note that C of the probe pads is implicitly de-embedded, and that the Q is given accurately up to the SRF - unlike the computation of Q found in many articles as X_L/R taken directly from measured data (which leads to Q=0 at SRF!).

current-crowding issue which predicts that wide traces should work best at low frequency, while narrow traces will have a higher critical frequency and may work better near SRF. To validate this prediction, a spiral was created using metal 3-6, as in the reference inductor, but with trace width decreased to 10um while holding trace pitch approximately constant. The results are shown on the right side of Figure 5. Note that the Q is significantly lower at low frequencies due to the higher DC resistance of the narrow traces, but is higher above about 1.2 GHz due to reduced current-crowding. Surprisingly, the SRF is only slightly increased - a fact that is partially explained by the increased inductance offsetting decreased turn-to-shield C.

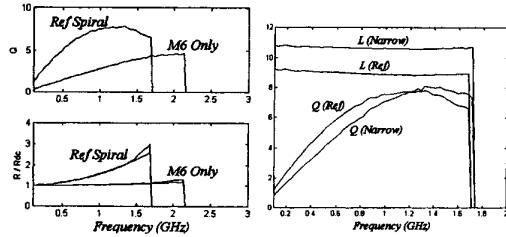


Figure 5. Performance vs reference spiral with metal-6 only (left) and with narrow traces (right). Values set to zero for $f > SRF$.

VI. GROUND-SHIELD PROS AND CONS

To validate the need for the ground-shield, a spiral was fabricated identical to the reference inductor, but with the shield removed. The results are shown on the left side of figure 6.

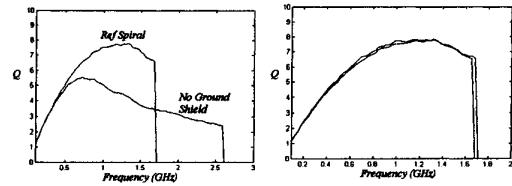


Figure 6. No ground shield (left) and ground shield with less dense patterning (right) compared to reference.

Although the shield does not provide much performance improvement below about 500 MHz (where I_{Cs} in Figure 1 is small), the benefits are indeed dramatic at higher frequencies as the reactance of C_{ls} tends toward the substrate resistance values R_{ls} [5]. In addition, the SRF is increased when the shield is omitted, due partly to increased oxide thickness, but primarily to the now, non-zero R_{ls} values. To see this, one can perform a series to parallel conversion on the $C_{ls} R_{ls}$ elements, which yields a

smaller effective C value. Unfortunately, this increased SRF comes at a significant price for this particular spiral inductor design.

In order to verify that the shield cuts used in the reference spiral are sufficiently dense to prevent substantial eddy currents, an additional spiral with a shield, but with cuts only every 30um was measured. The results are shown on the right side of figure 6. This plot verifies that the cuts are effective, leaving current-crowding as the dominant problem (under the assumptions that the shield Rsheet is sufficiently low and that substrate eddy currents are negligible).

VII. VIA DENSITY AND FILL METAL

The effects of reducing via density from a pitch of approximately 1um between vias to 8um between vias is shown on the left side of Figure 7. This result indicates that via density is not a critical factor, but that higher density does tend to increase Q slightly⁴. Note that it may, however, still be important to keep vias near the edge of the traces to deal with current crowding. In each case shown here, vias were placed within about 0.5 um of the trace edges.

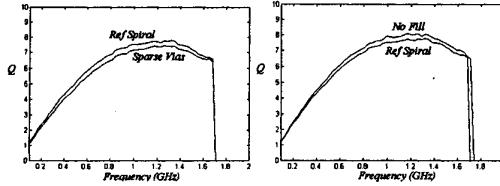


Figure 7. Effects of via density (left) and fill-metal (right).

Finally, the effects of fill-metal on spiral performance were investigated by comparing the reference spiral to a spiral created without fill-metal. As shown in figure 8, the reference spiral includes a moderate density fill pattern on all layers. This fill decreases the SRF slightly, presumably due to an increase in capacitance to the shield, but the metal "bricks" should be too small to introduce significant eddy current or other losses. The small decrease in Q at high frequencies is somewhat unexpected here and its cause is still under investigation.

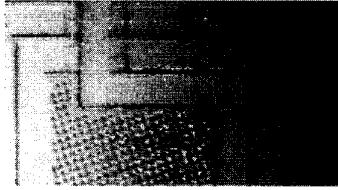


Figure 8. Photo of metal-fill pattern used in process.

⁴ This may depend somewhat on the type of vias used. Here, vias are plugs and metal layers are flattened through planarization.

VIII. CONCLUSIONS

Spiral inductors fabricated in bulk-CMOS with non-epi wafers and multi-level copper metalization can provide excellent Q at low frequency, but current-crowding problems degrade Q at higher frequencies. Experiments described in this study illustrate most of the important considerations in inductor design, including the effects of via density and metal-fill. Fortunately, it is found that modest-density metal-fill, being increasingly required in sub-micron processes, does not strongly affect spiral performance - a result that should make both designers and fabricators happy.

ACKNOWLEDGMENTS

The authors are very grateful to the Semiconductor Research Corporation, Novellus Corporation, and UMC Corporation for hosting the university SRC Copper Design Challenge and for fabrication of the chips in the UMC advanced copper process, which made this work possible. Additional support was provided by the National Science Foundation under grant ECS-9875770.

REFERENCES

- [1] J. R. Long, M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," IEEE JSSC, pp. 357-369, March 1997.
- [2] J. N. Burghartz, et.al., "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," IEEE Trans. MTT, pp. 100-104, Jan 1996.
- [3] J. N. Burghartz, et.al., "Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrates", IEEE IEDM, 1996.
- [4] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," IEEE Journal of Solid-State Circuits, pp. 743-752, May 1998.
- [5] W. B. Kuhn, and N. K. Yanduru, "Spiral Inductor Substrate Loss Modeling in Silicon RFICs," Microwave Journal, pp. 66 - 81, March 1999.
- [6] J. Craninckx and M. S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," IEEE Journal of Solid-State Circuits, pp. 736 - 744, May, 1997.
- [7] W. B. Kuhn and N. M. Ibrahim, "Analytical Modeling of Current Crowding Effects in Multi-turn Spiral Inductors," IEEE Trans MTT, pp. 31-38, Jan. 2001.
- [8] S. R. Kythakyapuzha and W. B. Kuhn, "Modeling of Inductors and Transformers", Proceedings of the 2001 IEEE RFIC) Conference, pp. 283-286, 2001.
- [9] Available through web page at www.eece.ksu.edu/vlsi